FIG. 1

100

102

106

108

109

126

124

110

122

130

114

128

112

116

120

118

FIG. 2

user data
CRC (cyclic redundancy code)
parity bits

210
305
P_1, P_2

210-1	210-2
210-4	210-3

300

Append CRC

	210-3

305

300

or

	210-3

305

300

Add single parity check

210-1		P_1
	210-3	
		P_2

P_1 P_1 305 P_2

300

or

210-1 [6] [1]	[4]	P_1
[3]	210-3 [2] [5]	
		P_2

P_1 P_1 305 P_2

300

Interleave and serialize

[1] [2] [3] [4] [5] [6] ...

FIG. 3-1

user data
CRC/ECC
parity bits

210
305
P_1, P_2

210-1	210-2
210-4	210-3

300

Append CRC

210-2	305
210-3	305

300

or

210-4	210-3	305
	305	

300

Add single parity check

P_1 305
P_1

210-2	305
210-3	

P_2 P_2

300

or

P_1 P_1

6 1	4	
210-4	3	2	210-3	5

305   305

P_2 P_2

300

Interleave and serialize

1 2 3 4 5 6 ...

FIG. 3-2

FIG. 3-3

user data 210

CRC/ECC 305

parity bits P_1, P_2

210-1	210-2
210-4	210-3

Append CRC →
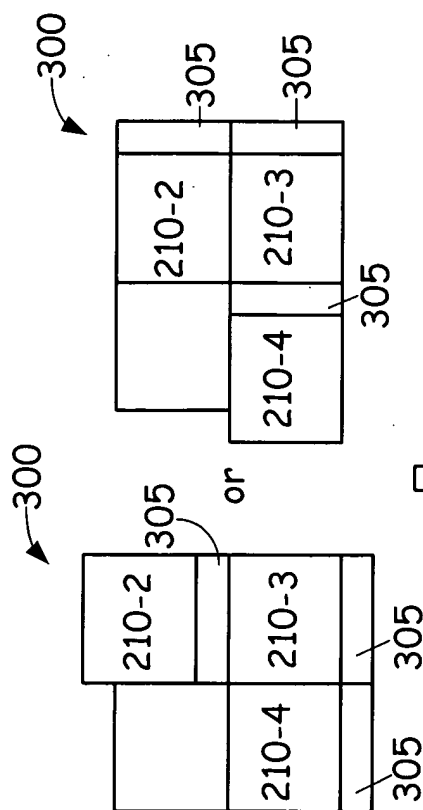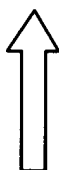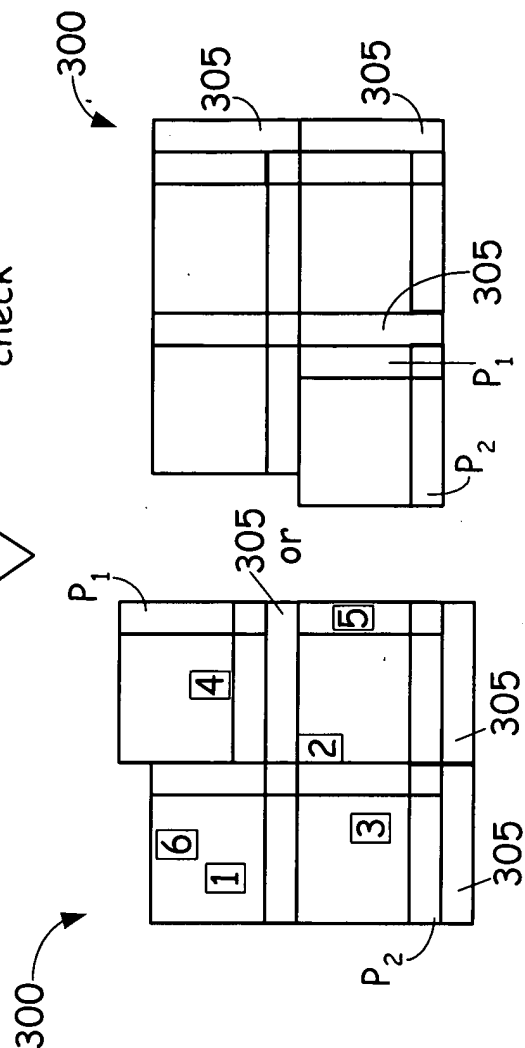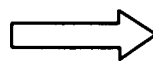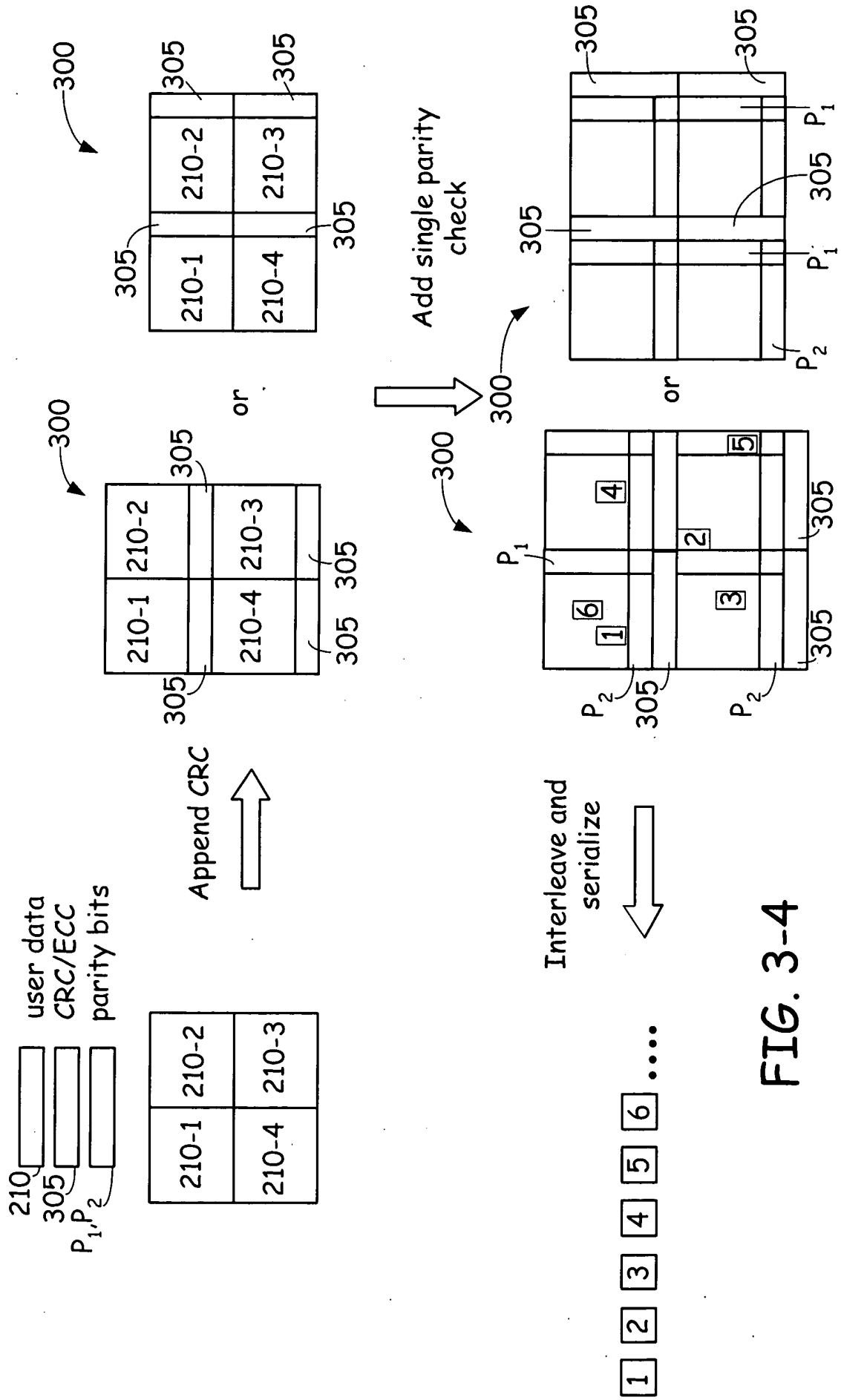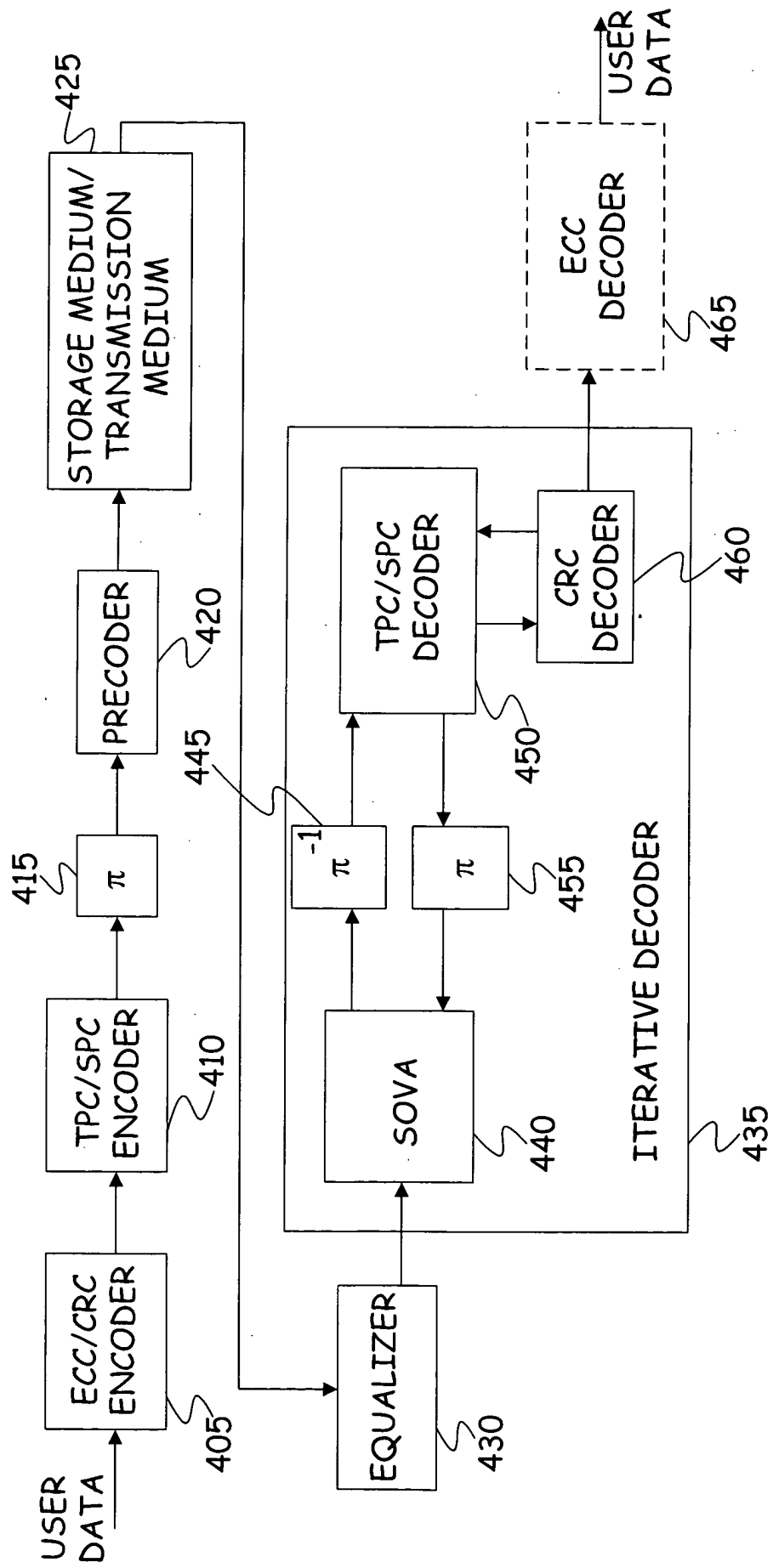
210-1	210-2
210-4	210-3
305 305

or

210-1	210-2
210-4	210-3
300
305 305 305

⇒ 300

Add single parity check

300

P_1

P_1

305 305

305

P_2

or

300

P_1

6 1	4
3	2 5

P_2 305 P_2

305 305

Interleave and serialize ↓

1 2 3 4 5 6 . . . .

FIG. 3-4

USER
DATA

STORAGE MEDIUM/
TRANSMISSION
MEDIUM

425

PRECODER

420

π

415

TPC/SPC
ENCODER

410

ECC/CRC
ENCODER

405

USER
DATA

ECC
DECODER

465

TPC/SPC
DECODER

450

CRC
DECODER

460

π
-1

445

π

455

SOVA

440

ITERATIVE DECODER

435

EQUALIZER

430

FIG. 4

DATA →

SOVA `540`

↓

Deinterleaver `545`

↓

TPC/SPC Decoder `550`

↓

CRC `560`

pass →

fail →

Max # of iterations reached? `570`

yes →

ECC Decoder `575`

no →

Interleaver `555`

MUX `565`
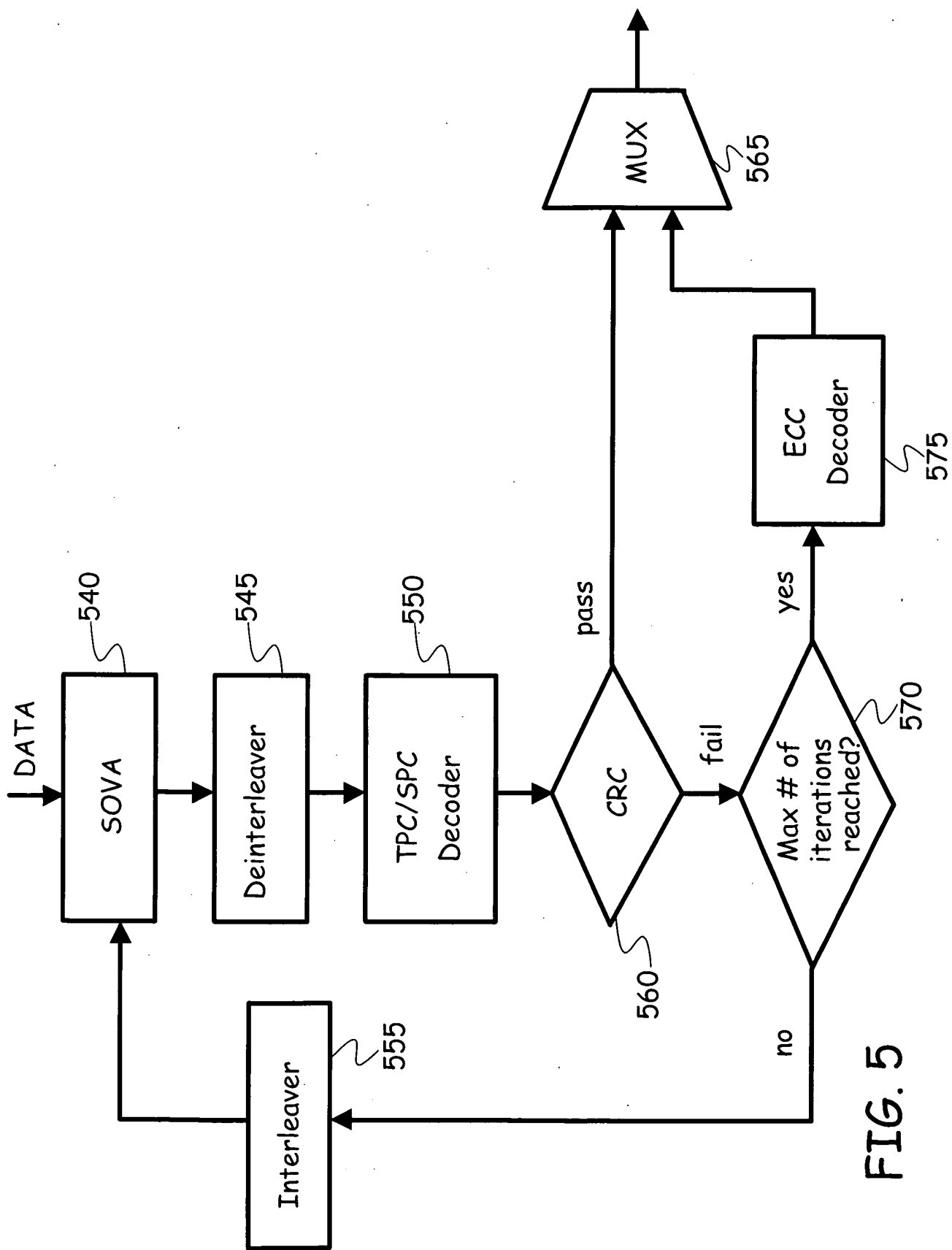
FIG. 5
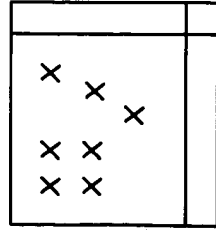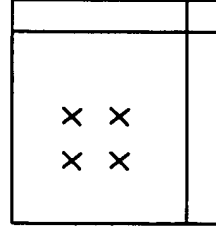
FIG. 6-1
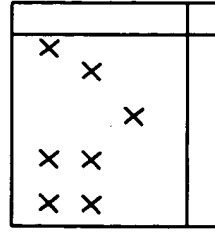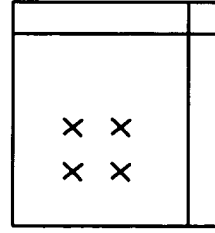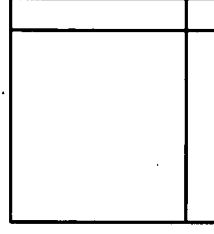
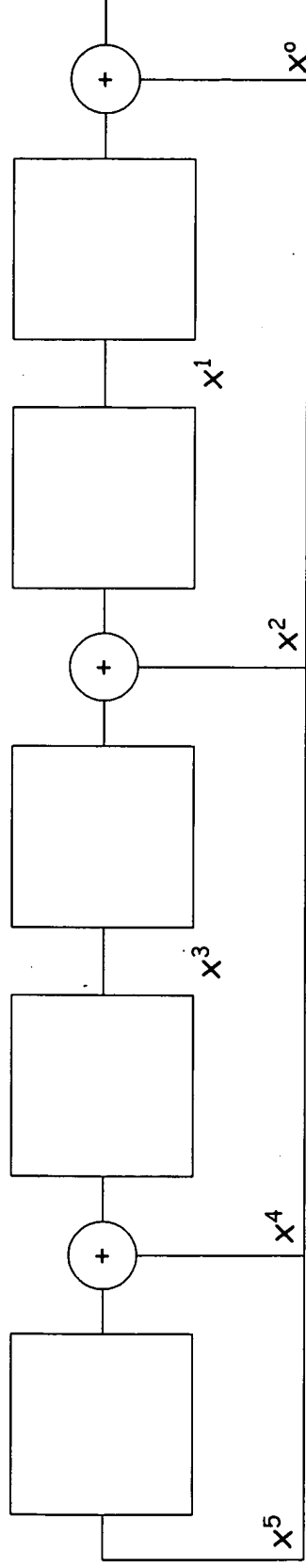x = error bit

FIG. 6-2

x = error bit

Input bits when creating CRC 1010001101000000

Input bits when creating CRC 1010001101010110

460

x^0

x^1

x^2

x^3

x^4

x^5

$P(x)=x^5+x^4+x^2+1$

FIG. 7

SNR = 6.4dB, 1600 codewords were simulated*

Termination Criterion	# of Error Events	# of wrong bits in those error events
Parity check Equation	44	4 10 4 14 6 2 4 4 4 4 1 8 4 4 6 8 4 1 4 4 4 6 12 2 4 2 4 4 4 4 2 10 3 4 4 4 4 6 4 4 8 4 4 1 4
CRC	5	1, 1, 2, 3, 1

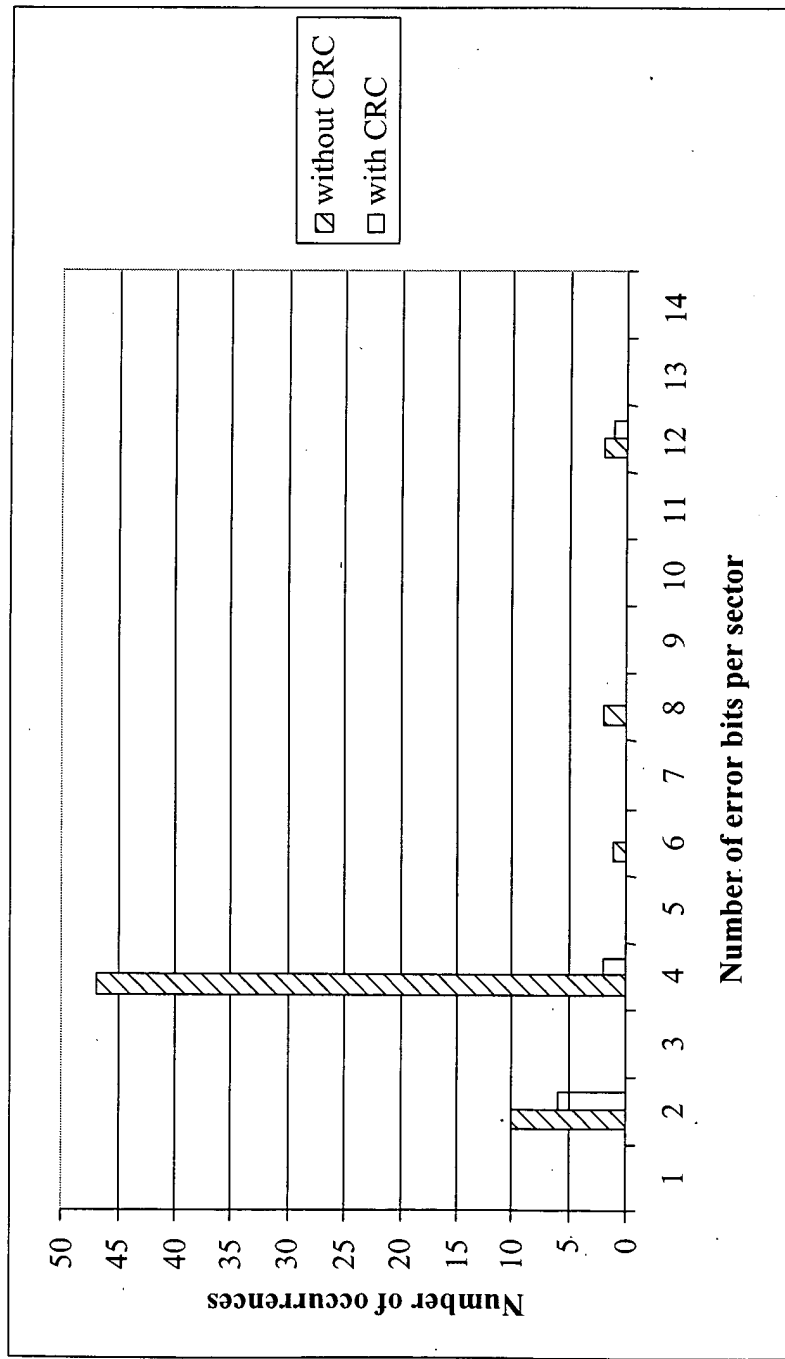*SOVA/TPCSPC system With fixed-point calculation.

FIG. 8

Number of occurrences

Number of error bits per sector

☒ without CRC
☐ with CRC

FIG. 9